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2–20-GHz GaAs Traveling-Wave Power Amplifier

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***Abstract*—Power amplification in FET traveling-wave amplifiers is examined, and the mechanisms which limit power capability of the amplifier are identified. Design considerations for power amplification are discussed. A novel single-stage and two-stage monolithic GaAs traveling-wave power amplifier with over 250-mW power output in the 2–20-GHz frequency range is described.**

I. INTRODUCTION

THE WIDE BANDWIDTH capability of distributed or traveling-wave amplifiers is well known [1]–[3]. Traveling-wave amplification by adding the transconductance of several FET's without paralleling their input or output capacitances looks very promising for achieving wide-band microwave amplification. Already 2–20-GHz decade band amplification with 30-dB gain has been reported with GaAs FET's in monolithic form [4]. The relative insensitivity of the amplifier performance with respect to transistor and circuit parameter variations, good input and output match, and stable operation of these devices makes them very attractive for future commercial and military applications. Because of these potential applications, the power performance of the device is also of great interest; however, to our knowledge this problem has not yet been addressed in the literature.

This work discusses the power-limiting mechanisms in a GaAs FET traveling-wave amplifier and describes a new circuit approach which decreases the effect of some of these limiting mechanisms. In particular, design and performance of a 2–20-GHz power amplifier are presented.

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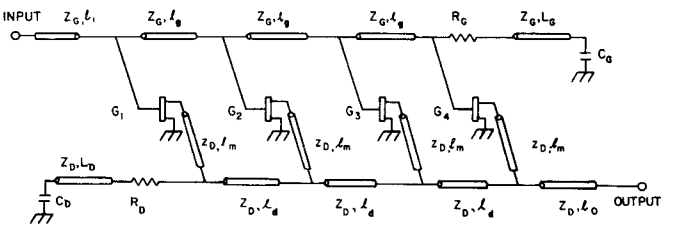

Fig. 1. Schematic representation of a four-cell FET traveling-wave preamplifier.

II. TRAVELING-WAVE POWER AMPLIFICATION CONSIDERATIONS

Schematic representation of a four-cell FET traveling-wave amplifier is shown in Fig. 1. The design considerations and microwave performance of such an amplifier with GaAs MESFET's as active devices have been described in our earlier paper [5], where it was shown that when drain losses are small compared with gate-line losses, the small-signal gain expression for the amplifier can be written approximately as

$$G = \frac{g_m^2 n^2 Z_0^2}{4}\left(1 - \frac{\alpha_g l_g n}{2}\right)^2 \tag{1}$$

where

g_m transconductance per FET,
n number of FET's,
Z_0 input and output characteristic impedance,
α_g effective gate-line attenuation per unit length,
l_g length of gate transmission line per unit cell.

This expression is derived using simplified circuit and device models. As such, it is not intended to be used as a design equation. However, despite its simplicity, (1) is very

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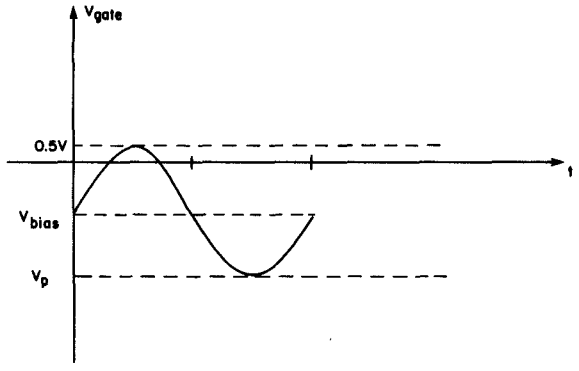

Fig. 2. Maximum RF voltage swing allowed on the gate line.

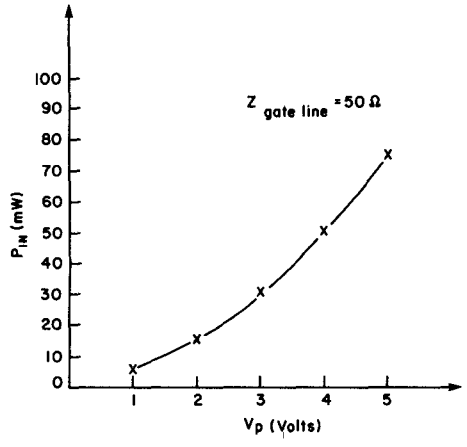

Fig. 3. Maximum allowable input power to a FET traveling-wave amplifier as a function of device pinchoff voltage.

useful in bringing out the effect of almost all the salient design parameters on the amplifier gain, allowing us to investigate various parameter tradeoffs. For a full circuit design, the analysis gets so complicated that computer-aided design techniques must be employed.

For power amplification, there are additional constraints. In fact, one can identify four separate power-limiting mechanisms in microwave traveling-wave power amplifiers.

In discussing these constraints, we will consider large-signal operation of FET's only in basic terms. Our intention here is to define the issues involved in distributed power amplification and identify the limiting mechanisms.

The first power-limiting mechanism is the finite RF voltage swing that can be allowed on the input gate line. This swing is limited on the positive RF cycle by the forward conduction of the gate and on the negative cycle by the pinchoff voltage of the device, as shown in Fig. 2. Hence, for a 50-Ω input impedance amplifier with −4-V pinchoff voltage FET's and, assuming the devices are biased at a drain current $I_{dss}/2$, the maximum input RF power to the amplifier is limited by

$$P_{\text{in,max}} \cong \frac{(4+0.5)^2}{8\times 50} = 0.051 \text{ W}.$$

Thus, maximum output power from the amplifier cannot be larger than Gain × $P_{\text{in,max}}$ under any circumstances. The

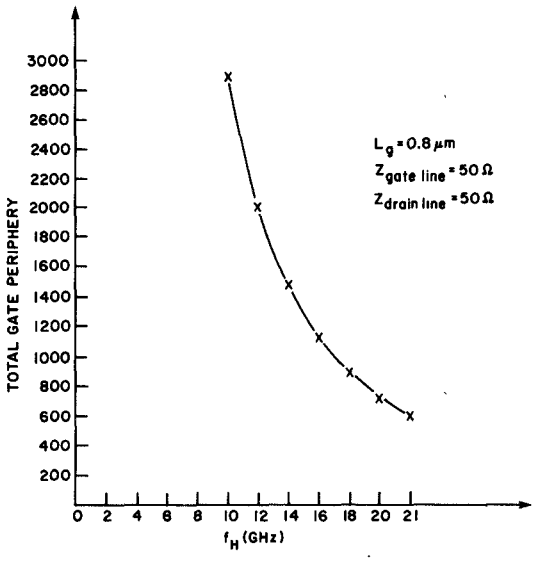

Fig. 4. Maximum total gate periphery per gain stage as a function of the highest frequency of operation.

quantity $P_{\text{in,max}}$ is plotted as a function of device pinchoff in Fig. 3.

The second power-limiting mechanism is the maximum total gate periphery that can be included in a single-stage design. Referring to (1), we note that the total attenuation on the gate line has to be kept below a certain value to maximize gain-per-stage per total FET periphery. In fact, from the simplified gain expression of (1), one can show that $\partial G/\partial n = 0$ at $\alpha_g l_g n = 1$. Other factors which also reduce gain but are not included in (1) frequently force the term $\alpha_g l_g n$ to be chosen less than 1. Hence, the following inequality has to be satisfied for a given design if one intends to employ the FET's in a single-stage design most efficiently:

$$\alpha_g l_g n \leqslant 1. \tag{2}$$

Relating the effective gate-line attenuation constant α_g to the FET input parameters r_g and C_{gs}, we find

$$r_g \omega^2 C_{gs}^2 Z_0 n \leqslant 2 \tag{3}$$

where

r_g gate resistance,
C_{gs} gate-source capacitance.

In (3), r_g varies inversely and C_{gs} varies directly with periphery for a given FET geometry. Hence, in terms of the periphery w per FET, (3) becomes

$$nw\omega^2 \leqslant \text{const.} \tag{4}$$

Thus, for a specified maximum frequency of operation and for a given FET, there is an upper limit to the maximum total periphery nw that can be employed in a single-stage design. This maximum periphery determines the gain and consequently the output power of a single-stage traveling-wave amplifier.

Fig. 4 shows the variation of maximum periphery per stage as a function of the highest frequency of operation f_H for a given 0.8-μm gate-length GaAs FET. Note that for

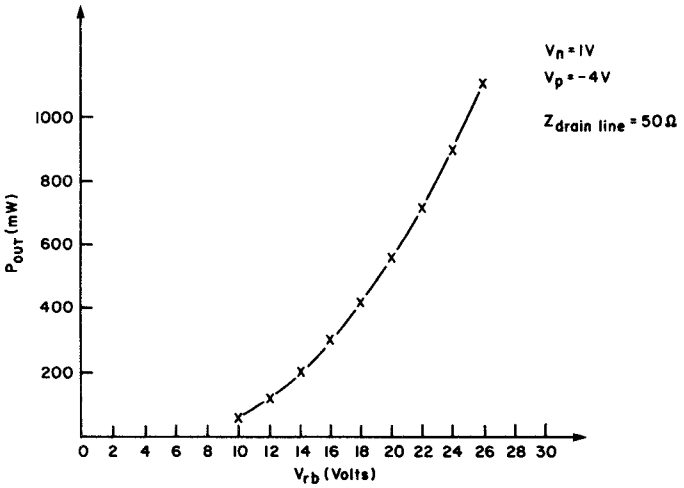

Fig. 5. Maximum output power for a GaAs FET traveling-wave amplifier as a function of gate drain reverse breakdown voltage.

this particular FET, maximum total stage periphery per stage is around 600 μm for $f_H = 20$ GHz.

The third power-limiting mechanism is the gate–drain breakdown voltage of the FET's. The drain terminals must be able to sustain the amplified RF voltage swings on the output transmission line. This voltage is given by

$$V_{\max}, \text{ peak-to-peak} \leqslant V_{\text{breakdown}} + V_{\text{pinch-off}} - V_{\text{knee}}. \quad (5)$$

Using this equation, the maximum saturated power output per stage of the amplifier can be calculated for a given output impedance. The results of such a calculation are plotted in Fig. 5.

Note from this figure that for a typical K-band FET with 15-V breakdown voltage, approximately 250 mW of output power can be expected. Our experience with actual amplifiers indicates that the values obtained from Fig. 5 are conservative.

Note that reduction of output impedance is not a clear-cut solution for increased output power because of the corresponding gain reduction associated with it.

The fourth power-limiting mechanism is related to the optimum ac load-line requirements. Fig. 6 illustrated the required optimum ac load line for class A operation of a discrete FET. For a traveling-wave amplifier, the load line that each individual FET sees is predetermined by the drain-line characteristic impedance, the only flexibility left in the design is the periphery of the unit FET. However, the total periphery is also predetermined from gate-loading considerations. For example, we have established that the total periphery allowed is around 600 μm for the 2–20-GHz amplifier. Hence, for the four-cell design, each FET has a 150-μm periphery. A typical optimum load line R_L for such a device is 280 Ω, representing a significant mismatch to a 50-Ω range output impedance.

Such an impedance mismatch has a significant effect on the output power and consequently on the efficiency of the amplifier stage. Assuming that maximum gain per stage $G_{\max}$ is always less than $g_m^2 n^2 Z_0^2/4$ (see (1)), the maximum theoretical limit for the power-added efficiency of the amplifier can be calculated. It can be shown that this

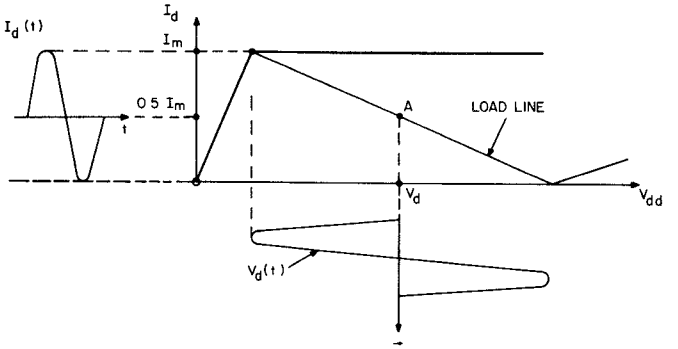

Fig. 6. The required optimum ac load line for class A operation of a discrete FET.

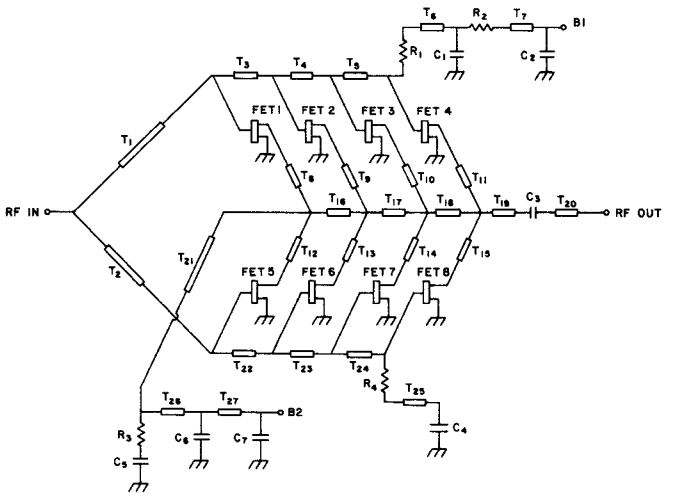

Fig. 7. Power amplifier with eight 150-μm unit cells.

theoretical maximum value is

$$\eta_{\text{power added}_{\max}} < \left(1 - \frac{1}{G}\right)\frac{1}{8} n \frac{Z_0}{R_L}. \quad (6)$$

Equation (6) indicates that increased periphery per stage helps to increase efficiency if this increased periphery does not adversely affect the gain at f_H.

On the basis of this analysis of power amplification in traveling-wave amplifiers, we will next describe a novel approach for increased power.

III. Traveling-Wave Power Amplifier Design

Some of the problems outlined above have been addressed in the development of 2–20-GHz power amplifiers. Consider the power amplifier circuit design shown in Fig. 7. In this circuit, the adverse effects of three of the mechanisms identified as limiting the maximum output power are reduced.

First, the input power is equally divided into the gate lines, each employing 4×150-μm FET's, using a Wilkinson power divider without the isolation resistor; we are able to obtain decade bandwidth performance from a single-section Wilkinson divider because of the good input match characteristics of the amplifiers.

Second, the FET's excited from two separate gate lines are combined on a single drain line, effectively giving a

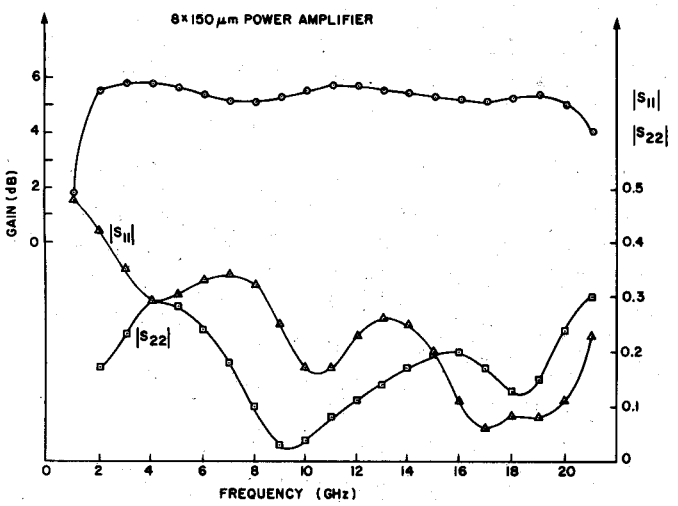

Fig. 8. The predicted performance of the traveling-wave power amplifier in the 2–20-GHz frequency range.

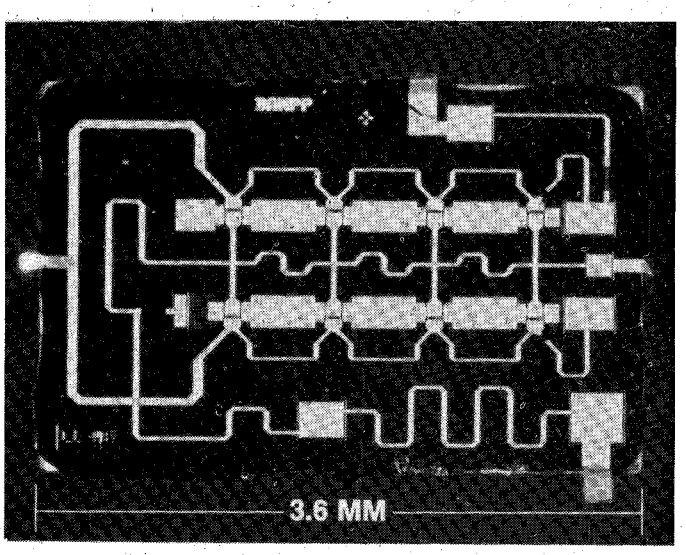

Fig. 9. Single-stage 2–20-GHz power amplifier chip.

4×300-μm drain periphery. Thus, the total gate periphery is doubled without affecting the loading on the gate lines. In this way, the gate loading is limited to a 600-μm gate periphery, whereas the output power will be determined by a 1200-μm drain periphery.

Third, the required load-line impedance is halved, since we have twice the drain periphery on the output line. This brings its value closer to the optimum load-line impedance. Since gain per stage is not significantly affected, the efficiency of the amplifier is effectively doubled.

This amplifier configuration does nothing for the drain-line voltage breakdown problem. However, in this particular design, the improvements outlined above are able to bring the output power only to the point where drain-line breakdown will start to be a limiting factor. Hence, the circuit is optimized with respect to all the constraints described above. In the design, -4-V pinchoff voltages are assumed for the FET's. This allows 50-mW input power per gate line and twice that for the amplifier. With 5-dB small-signal gains, approximately 300 mW can be expected at the output. Drain-line breakdown effects should start showing up at around 250-mW output power levels, with gate–drain breakdown voltages in the 15-V range.

The predicted performance of the amplifier designed for 50-Ω input/output impedance is shown in Fig. 8. Gain is 5 ± 0.5 dB. Input and output return loss is in the neighborhood of 10 dB at all frequencies except at 2 GHz, where the input return loss is only 7 dB. The increased input mismatch at the low end is due to the fact that the input impedance transformer is becoming less and less effective as its electrical length gets smaller and smaller at the low end of the band.

A dc blocking capacitor is included in the design of the output drain line. This amplifier is intended as one of the stages in a chain of cascaded amplifiers. Hence, dc blocking on one side of the amplifier is sufficient.

The two-stage version of this amplifier is also designed with a five-FET stage driving the power stage, with a total of 10-dB small-signal gain.

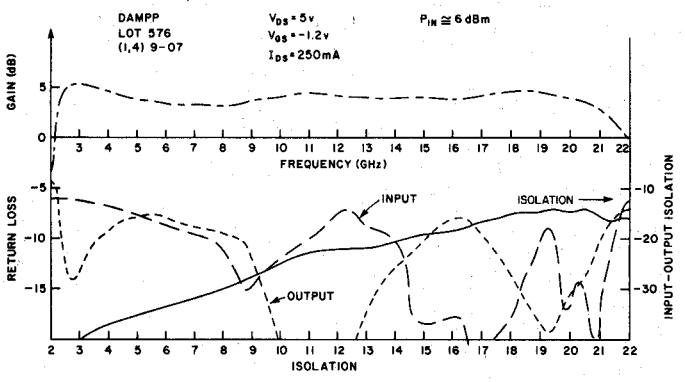

Fig. 10. Measured small-signal performance of the 2–20-GHz power amplifier.

IV. Experimental Performance

A photograph of the finished single-stage power amplifier chip is shown in Fig. 9. The chip size is 2.31×3.64 mm (91×143 mils) on 0.1-mm (4-mil) GaAs substrate.

Thin-film capacitors on the chip add up to a total of 34 pF. The dielectric material is plasma-enhanced CVD silicon nitride. The thin-film resistor material is titanium; it is evaporated by electron beam and patterned by photoresist liftoff.

The total gate periphery on the chip is 1200 μm. The amplifier design was completed using 0.8-μm gate-length, -4-V pinchoff voltage FET models. However, the actual gates on the wafer turned out to be 1 μm long.

The measured small-signal performance of the amplifier is shown in Fig. 10. Its gain is 4 ± 1 dB in the 2–21-GHz frequency band, which is about 1-dB lower than predicted. The input and output return loss curves are about 2 dB higher than predicted.

Despite the lower gain, the amplifier achieved over 250-mW power output in the 2–20-GHz frequency band. Power performance of the amplifier is shown in Fig. 11. Power-added efficiencies in the 7–14-percent range have been recorded.

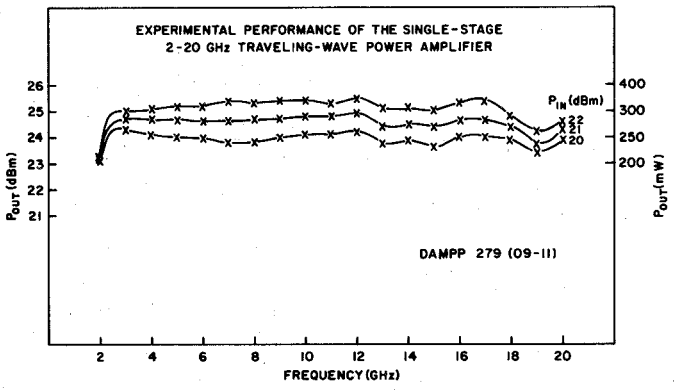

Fig. 11. Experimental power performance of the 2–20-GHz amplifier.

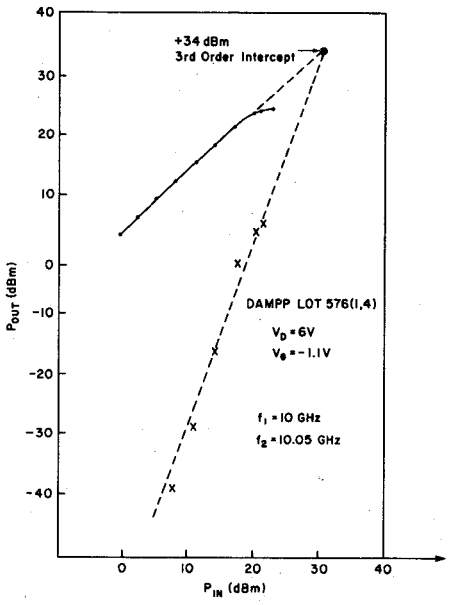

Fig. 12. Third-order intermodulation measurement results at midband.

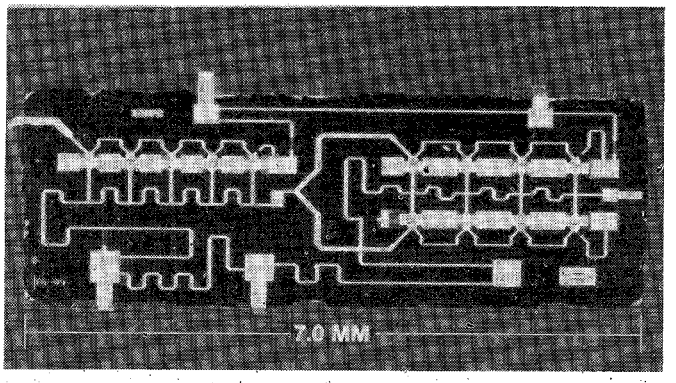

Fig. 13. Two-stage amplifier chip.

Third-order intermodulation products for the amplifier have also been measured. Fig. 12 shows the measured data at midband. The intercept point is at +34 dBm.

Fig. 13 is a photograph of the two-stage chip. The chip size is 2.31×6.95 mm (91×274 mils). Total gate periphery is 1950 μm with thirteen 150-μm FET's. Both stages are biased from a single-gate and a single-drain bias terminal. A typical bias point would be −1 V on the gates with +6 V on the drains.

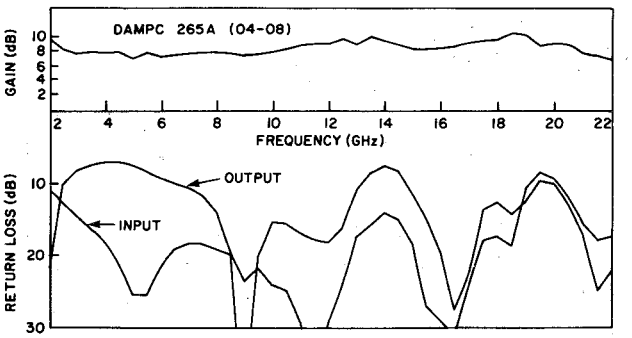

Fig. 14. Two-stage power amplifier gain and return loss performance in the 2–22-GHz frequency band.

Experimental performance is 9 dB±2 dB in the 2–21-GHz frequency range, as shown in Fig. 14. The gain is 1-dB lower than the predicted gain of 10.25±1.25 dB in the same frequency band.

V. Conclusion

A GaAs traveling-wave microwave amplifier is examined in terms of its large-signal power amplification capabilities; several mechanisms which may limit the output power are identified. A new circuit configuration which doubles the output power of the amplifier is described in relation to a 2–20-GHz power amplifier design. The experimental performance of the amplifier with 4-dB and 9-dB gain and over 250-mW power output is presented.

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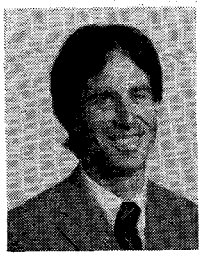

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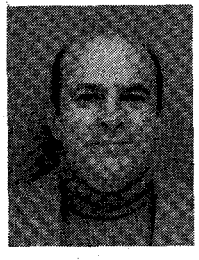

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From 1963 to 1967, he attended the Massachusetts Institute of Technology under a Raytheon advanced study grant. His studies at MIT culminated in a thesis on an *X*-ray diffraction study of the structure of glass. He was awarded his Ph.D. in physics in February 1968.

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In 1971, he began exploratory studies on the applications of ion implantation for the impurity doping of semiconductor devices. These studies led to the establishment of an ion implantation laboratory at the Research Division. He has been responsible for the operation of this facility, which includes a 400-kV heavy ion accelerator, and for the Division's ion implantation studies.

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